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RM-6489

B. E. - II (EC / ECC) (Sem. - IV) Examination

May / June – 2010

Digital Circuits

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.
Name of the Examination :
☛ **B. E. - 2 (EC / ECC) (SEM. - 4)**
Name of the Subject :
☛ **DIGITAL CIRCUITS**
☛ Subject Code No. : **6 4 8 9** ☛ Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Assume suitable data whenever found necessary.
(3) Figures to the right represent marks.
(4) All notations have their usual meanings.
(5) Figure diagram must be neat and clean.
(6) Programmable calculators are not allowed.

SECTION– I

1 (a) Attempt the following : **10**

(1) The Boolean function $Y = AB + CD$ is to be realized using only 2-input NAND gates. The minimum number of gates required is

(A) 2
(B) 3
(C) 4
(D) 5

(2) Which of the following is incorrect ?

(A) $(8)_{16} = (8)_8$

(B) $(5)_{16} = (5)_8$

(C) $(10)_2 = (2)_{10}$

(D) $(2)_{16} = (2)_{10}$

(3) 4-bit 2's complement representation of a decimal number is 1000. The number is

(A) +8

(B) 0

(C) –7

(D) –8

(4) The Boolean function $x'y'z'+xy'z'+x'yz'+xyz'$ is equivalent to

(A) $x'y$

(B) xy'

(C) z'

(D) y'

(5) $(11011)_2$ in gray code = (_____)

(A) 10010_2

(B) 11111_2

(C) 11100_2

(D) 10001_2

(b) Define the following terms : **2**

(1) Combinational circuit

(2) Self complementary code

(c) $(231)_4 \times (13)_4 = (?)_4$ **2**

(d) State the rule for BCD substraction. Do the following BCD substraction using 9's complement method : **6**

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2 (a) Find the minimum sum - of - product and product - of - sum forms for the following using k-map : **6**

(1) $Y(A, B, C, D) = (A+B'+D)(A'+B+D)(C+D)(C'+D')$

(2) $Y = x'z'+y'z'+yz'+xyz$

(b) Design and draw the circuit for BCD to seven segment code converter. **9**

OR

2 (a) Design a code converter which converts 8 4 – 2 – 1 BCD code into BCD code. **6**

(b) It is necessary to multiply two binary nos. each two bits long, in order to form their products in binary, Let the two no. be represented by a1, a0 and b1, b0 where subscript 0 denotes LSB. Find the simplified Boolean expression for each output. **9**

3 Attempt any **three** : **15**

(a) Explain and draw the circuit for BCD adder using binary parallel adder IC.

(b) Design Octal to Binary encoder.

(c) Explain look ahead carry generator.

(d) Design a 4-line to 2-line priority encoder. Include an output E to indicate that atleast one input is a one.

SECTION– II

4 (a) Answer the following questions : **10**

(1) Application of the flip-flop. **2**

(2) State the difference between Edge-triggered and level triggered flip-flop. **1**

(3) What is lock-out condition in counter ? **1**

(4) What is buffer register ? Draw the logic diagram of 4-bit buffer register ? **2**

(5) Advantages and disadvantages of the synchronous counters ? **1**

(6) "MUX can be used as a logic function generation". Determine the statement whether it is true/false with reason. **1**

(7) What is race around condition ? **1**

(8) Define ring counter and switch-tail counter ? **1**

(b) Implement a full adder circuit with 4×1 MUX. **5**

(c) Design SR flip-flop using JK flip-flop. **5**

5 (a) Explain Bi-directional shift register in detail. **7**

(b) Modify a 3-bit linear sequence generator to output 4-states. **8**

OR

5 (a) Design and implement a mod-10 asynchronous counter using T flip-flop. 8

(b) Explain 3-bit odd parity bit generator. 7

6 Attempt any **three** : 15

(1) Johnson counter

(2) Explain master sleeve flip-flop constructed from two R-S flip-flop.

(3) Explain with logic diagram of 4-bit parallel-in, serial out, shift register.

(4) Design a J-K counter that goes through state 3, 4, 6, 7 and 3..... Is the counter self-starting ? Modify the ckt. such that whenever it goes to an invalid state it comes back to state 3.